# LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING
## (AUTONOMOUS)
L.B. Reddy Nagar :: Mylavaram-521 230 :: NTR Dist. :: A.P
Approved by AICTE, New Delhi. Affiliated to JNTUK, Kakinada

## M.Tech. (I Semester) (R23) Semester End Examinations (Supplementary) – March 2026

## TIME TABLE

**R23**

**Time : 10.00 AM to 01.00 PM** **A.Y. : 2025-26**

| Specialization | 09-03-2026 (Monday) | 10-03-2026 (Tuesday) | 11-03-2026 (Wednesday) | 12-03-2026 (Thursday) | 13-03-2026 (Friday) |
|---|---|---|---|---|---|
| | | | Program Elective-I | Program Elective-II | |
| Data Science | 23DS01 - Statistical Foundations for Data Science | 23DS02 - Machine Learning | 23DS03 - Cloud Computing and Virtualization | 23DS07 - Social Media Analytics | 23RM01 - Research Methodology and IPR |
| Power Electronics and Electrical Drives | 23PE01 - Analysis of Power Converters | 23PE02 - Control of Motor Drives-I | 23PE03 - Power Quality | 23PE08 - Meta Heuristics Optimization Techniques<br>*23PE06 - Modern Control Theory* | 23RM01 - Research Methodology and IPR |
| VLSI and Embedded Systems Design | 23VE01 - Digital VLSI System Design | 23VE03 - Cryptography and Network Security | 23VE02 - Embedded System Design | 23VE06 - Image and Video Processing | 23RM01 - Research Methodology and IPR |

Note: Any omissions or clashes in the time table may please be informed to the Controller of Examinations immediately.

**Date: 21-02-2026** **CONTROLLER OF EXAMINATIONS** **PRINCIPAL**

Copy to: 1. Vice-Principal, Deans & HoDs 2. T&P cell, Transport in-charge & Librarian
3. Canteen, PD, Security & Hostels 4. Coordinator-Disciplinary 5. Notice Boards

| H.T.No | | | | | | | | | | |
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09 MAR 2026

R23

**LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING (AUTONOMOUS)**

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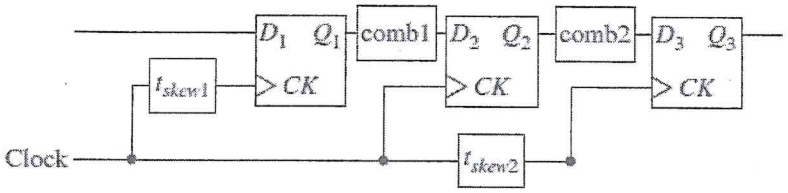
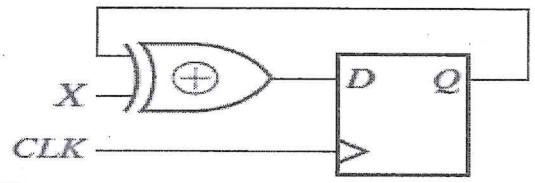
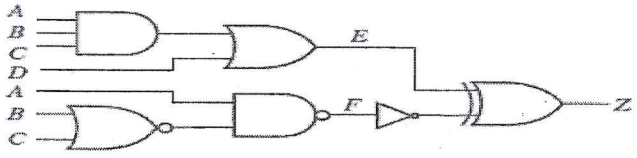
M.Tech. (I Semester) ~~Regular~~/Supplementary Examinations

**23VE01-DIGITAL VLSI SYSTEM DESIGN**

(VLSI&ESD)

Time : 3 hours Max. Marks : 60

| Q.No | All questions carry equal marks | Marks | CO | BL |
|---|---|---|---|---|
| 1(a) | Mention the different ways of simplifying a logic expression using the theorems. | 6M | CO1 | L2 |
| (b) | Calculate minimum clock period with $t_{skew1}$ = 0; $t_{skew2}$ = 3. Is the setup time and hold-time violated for the middle flip-flop when set Tcomb1 = 1 to 4 ns. If no, examine is the setup time margin for the following circuit where the combinational circuit.<br>Given the parameters: setup time = 10 ns;<br>hold time = 2 ns; propagation delay = 12 to 20 ns<br>Tcomb-1 = 5 ns to 7 ns; Tcomb-2 = 6 ns to 11 ns<br>  | 6M | CO1 | L3 |
| | **(OR)** | | | |
| 2(a) | summarize the steps required to design a sequential circuit. | 4M | CO1 | L2 |
| (b) | Calculate the minimum clock period for proper operation of the circuit, and the earliest& latest times after the rising clock edge at which X is allowed to change for the following circuit, with XOR gate delay in the range of 2 to 16ns. The D flip-flop propagation delay from clock to Q in the range 12 to 24ns. The setup time is 8 ns, and the hold time is 4 ns.<br>  | 8M | CO1 | L3 |
| 3(a) | List out the important coding practices while writing synthesizable Verilog for sequential hardware. | 6M | CO2 | L2 |
| (b) | Model the Verilog description for the following combinational circuit using concurrent statements. Each gate has a 5-ns delay, excluding the inverter, which has a 2-ns delay.<br>  | 6M | CO3 | L3 |
| | **(OR)** | | | |
| 4(a) | Construct Verilog code that finds the largest register in the array-A of 20 4-bit registers using 'for loop' and 'while loop'. | 6M | CO3 | L3 |
| (b) | Develop Verilog module that implements an M-N flip-flop responds to the falling clock edge as follows:<br>M N Output<br>0 0 changes state<br>0 1 set to 1<br>1 0 set to 0<br>1 1 no change<br>The flip-flop is cleared asynchronously if *CLRn* = 0. | 6M | CO4 | L3 |

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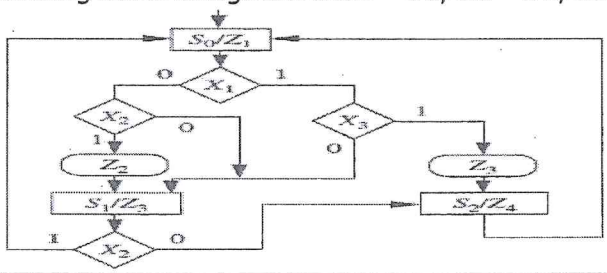
|---|---|---|---|---|
| 5. | Create Verilog Code for a sequential traffic light controller for the intersection of street "A" and "B." Sa =Sb =1 means a vehicle is approaching on street "A," and street "B." Street "A" has a green light until a car approaches on "B." Then the lights change, and "B" has a green light. At the end of 50 seconds, the lights change back unless there is a car on street "B" and none on "A," in which case the "B" cycle is extended for 10 additional seconds. If cars continue to arrive on street "B" and no car appears on street "A," "B" continues to have a green light. When "A" is green, it remains green at least 60 seconds, and then the lights change only when a car approaches on "B." | 12M | CO4 | L4 |
| | **(OR)** | | | |
| 6(a) | Develop Behavioral Model for 4 × 4 Binary Multiplier that It multiplies a 4-bit multiplicand by a 4-bit multiplier to give an 8-bit product. | 6M | CO3 | L3 |
| (b) | Draw a logic circuit with a 10-bit counter, 2-bit register N, all necessary gates, flip-flops and four pushbuttons (B0, B1, B2, and B3). Whenever a button is pushed, it is debounced, after which the circuit loads the button number in binary into 2-bit register (N) and holds value until another button is pushed. | 6M | CO4 | L3 |
| | | | | |
| 7. | Design a behavioral Model for Dice-Game Controller with the following rules:<br>(i). After the first roll of the dice, the player wins if the sum is 7 or 11. The player loses if the sum is 2, 3, or 12. Otherwise, the sum the player obtained on the first roll is referred to as a point, and he or she must roll the dice again.<br>(ii). On the second or subsequent roll of the dice, the player wins if the sum equals the point, and he or she loses if the sum is 7. Otherwise, the player must rollagain until he or she finally wins or loses. | 12M | CO4 | L4 |
| | **(OR)** | | | |
| 8(a) | Derive the next state and output equations for the following ASM chart, assuming the following state assignment:*S*0 =00, *S*1 =01, *S*2 = 10.<br>  <br> | 6M | CO4 | L3 |
| (b) | Draw the SM chart for the controller (three states) to implement a multiplier for 16-bit binary integers and add a counter to the control circuit to count the number of shifts. Assume that the counter outputs *K* =1 after 15 shifts have occurred. | 6M | CO3 | L2 |
| | | | | |
| 9(a) | Interpret the Verilog function that will create the 2's complement of an *N*-bit vector. Use a call of the form comp2 (bit_vec, N), where 'bit_vec'is the vector and *N* is the length of the vector. | 6M | CO3 | L2 |
| (b) | Develop a MIPS assembly language program for the following pseudo code segment:<br>for(i = 0; i < 100; i++)<br>y(i) = a * x(i) + y(i) | 6M | CO3 | L3 |
| | **(OR)** | | | |
| 10(a) | Create structural Verilog code for a module that has two inputs: an N-bit vector A, and a control signal B (1 bit). The module has an N-bit output vector, C. When B = 1, C <= A. When B = 0, C is all 0s. Use parameter to specify the value of N (default = 4). | 6M | CO3 | L3 |
| (b) | Examine the following MIPS instruction for what do the mentioned hexadecimal (hex) numbers correspond to? If it is not any instruction of correct format, denote it as an illegal opcode.<br>(i) 33333300 (ii) 8D8D8D8D (iii) 1777FF00 (iv) BDBD00BD (v) 01010101. | 6M | CO2 | L2 |

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11 MAR 2026

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R23

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M.Tech. (I Semester) ~~Regular~~/Supplementary Examinations

**23VE02-EMBEDDED SYSTEM DESIGN**

(VLSI&ESD)

Time : 3 hours Max. Marks : 60

| Q.No | All questions carry equal marks | Marks | CO | BL |
|---|---|---|---|---|
| 1(a) | Explain the Embedded system overview with digital camera example. | 6M | CO1 | L2 |
| (b) | Differentiate various processors technologies with neat schematics. | 6M | CO1 | L2 |
| | **(OR)** | | | |
| 2(a) | Describe resister transfer (RT) level combinational logic with an example. | 6M | CO1 | L2 |
| (b) | Discuss state encoding and state minimization in optimizing the FSM of single purpose processor. | 6M | CO1 | L2 |
| | | | | |
| 3(a) | Demonstrate the steps involved in implementation of concurrent processes. | 6M | CO2 | L3 |
| (b) | Illustrate the message passing method for communication among processes. | 6M | CO2 | L3 |
| | **(OR)** | | | |
| 4(a) | Explain the role of monitors in synchronization among the processes. | 6M | CO2 | L2 |
| (b) | Summarize the features of windows CE and QNX in operating systems. | 6M | CO2 | L2 |
| | | | | |
| 5(a) | Describe the principle features of the ARM architecture. | 6M | CO3 | L2 |
| (b) | Outline the ARM development tools and explain the features of each tool. | 6M | CO3 | L3 |
| | **(OR)** | | | |
| 6(a) | Examine the ARM control flow instructions set with an example. | 6M | CO3 | L2 |
| (b) | Write ARM assembly language program to subtract two 64 bit numbers. | 6M | CO3 | L3 |
| | | | | |
| 7(a) | Illustrate ARM branch instruction execution process with neat schematics. | 6M | CO4 | L3 |
| (b) | Discuss the ARM6 ALU organization with neat diagram. | 6M | CO4 | L2 |
| | **(OR)** | | | |
| 8. | Outline the each block of 3-stage pipeline ARM organization and list out its features. | 12M | CO4 | L3 |
| | | | | |
| 9(a) | Summarize the importance of each step involved in the IC manufacturing steps. | 6M | CO5 | L2 |
| (b) | List and describe three general approaches to improving designer productivity | 6M | CO5 | L2 |
| | **(OR)** | | | |
| 10(a) | Discuss about the RT and behavioral synthesis. | 6M | CO5 | L2 |
| (b) | Illustrate the new challenges posed by cores to processors providers. | 6M | CO5 | L3 |

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